IN THE SPECIFICATION:

Please replace paragraph 00021 with the following:

[00021] Reference is now made to Figure 1b which shows the timing signals for the circuit of Figure 1 in the case where a synchronisation error may occur. If there is a change, for example from 1 to 0 or from 0 to 1, in the input to the first flip-flop FF1, then the output of the first flip-flop FF1, labelled Q1, will change shortly after the rising clock edge of the first clock, Clock 1. The time taken for this change to be fully effected is known as the output delay time, which, when FF1 is operating within its specified limits, will have a value between a maximum time Tod (max) and a minimum time Tod (min) after the rising clock edge. Although the transition is a clean transition, from 0 to 1 or from 1 to 0, the precise timing of this transition cannot be determined and for this period, the signal Q1 may be described as undefined and given the label 'X'.

IN THE DRAWINGS:

Please replace Figures 1a, 1b, 2a, and 2b, with the replacement figures on the two attached replacement sheets.